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Code No: A5706

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH I SEMESTER EXAMINATIONS, APRIL/MAY-2012
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(VLSI SYSTEM DESIGN)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
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1.a) Distinguish between ALTERA's CPLD and CYPRESS Flash 370 device.
b) Compare the AMD's CPLD match 1 to 5.

2.a) Show the PLA implementation of a Binary adder of 4 bit.
b) Explain about the ALTERA's third generation architecture of MAX7000 family with neat diagram.

3.a) Explain about the alternative realization for state machine using micro programming.
b) Explain about the top-down design approach of state machine with an example.

4.a) Explain about one hot state machine with state table and state diagrams.
b) Develop one hot state diagram for a sequence checker whose output is '1' whenever the sequence 0101 is detected. Also specify its Transition Table.

5.a) Explain the extended petrinets for parallel controllers
b) Explain about linked state machine for a dice game.

6.a) Explain about the datapath and functional partition of FSM system level design
b) Design a binary multiplier control using one-hot method.

7. Explain the complete design flow to implement a 4 bit Ripple-carry adder circuit on to FPGA using an EDA tool. Also explain the timing simulation for the same.

8. Write a brief note on any two:
a) Floor plan
b) Optimized reconfigurable cell array.
c) Speed performance of different CPLDs.

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